IN THE SPECIFICATION

Please replace the paragraph beginning on page 1, lines 9-17 with the following rewritten paragraph:

"The original 8051 was a very simple machine, with a limited instruction set. The DS87C550 provides an extension of the original 8051, while maintaining compatibility with the original 8051 (i.e. the DS87C550 executes 8051 programs with the same effect as the 8051). The extension concerns the data pointer register of the original 8051. The original 8051 had a single data pointer register DPTR. The DPTR register is used in MOVE instructions to move data between register and memory locations. The DPTR contains an address that the processor uses to address memory used in the MOVE instructions. Data from a succession of addresses can be moved to register and processed by executing successive MOVE instructions, each followed by incrementation of the address in the DPTR register."

A1

Please replace the paragraph beginning on page 1, lines 18-22 with the following rewritten paragraph:

"The 8051 had a DPTR increment instruction INC for incrementing the DPTR. But the 8051 did not have the possibility to decrement the DPTR. The DS87C550 improves this. The DS87C550 introduces an instruction-settable control bit which controls whether the processor responds to the 8051 DPTR increment instruction by incrementing the DPTR or by decrementing the DPTR."

A2

Please replace the paragraph beginning on page 1, line 23 to page 2, line 2 with the following rewritten paragraph:

"The original 8051 only had a single DPTR register. If the original 8051 had to transfer data from a first series of memory locations to a second series of memory locations with MOVE instructions, the address in the DPTR register had to be replaced alternately with an address for addressing the first series and an address for addressing the second series. This caused considerable instruction overhead. The Dallas DS87C550 reduces this overhead. Two registers are provided instead of the single DPTR, one register for addressing memory in moves to memory and one for move from memory. In a toggle mode, the DS87C550 uses alternately one register and the other, e.g. in MOVE or INC instructions."

A3

Please replace the paragraph beginning on page 4, lines 18-24 with the following rewritten paragraph:

"The fourth instruction causes the processing device to move a value of 2 into the selector register. This value causes the processing device to receive the second address when a value is loaded subsequently into the data pointer register DPTR. The fifth instruction commands the move of an address value A1 to the data pointer register DPTR. Because the selector register has been set to 2, the processing device will use this address value A1 as the second address. Subsequently, the processing device will use alternately the first and the second address (updated if necessary) when memory access instructions refers to the DPTR."

A4

Please replace the paragraph beginning on page 5, lines 11-17 with the following rewritten paragraph:

"In operation the execution unit 10 executes a sequence of instructions. Each time that such an instruction refers to a data pointer register for specifying a memory address for memory access, the execution unit supplies an address enable signal on the address enable output to the address selector circuit. The register selector register 128 controls which one of the registers 120, 122 receives this address enable signal. This control is effect via the AND gates 124, 126. The enabled register 120, 122 will supply its content as an address to the address output of the processing device."

A5

Please replace the paragraph beginning on page 7, lines 1-11 with the following rewritten paragraph:

"Of course, implementation of the invention is not limited to the embodiment shown in figure 1. For example, instead of connecting both registers to the address output and enabling different ones of these registers 120, 122, one may place these registers in a circular shift register arrangement. In this shift register arrangement the content of the first register 120 is loaded into the second register 122, and the old content of the second register 120 is loaded into the first register 120 each time after the execution unit 10 supplies an address enable signal. Thus, only the first register 120 needs to be connected to the address output and the content of the first register is always output in case of an address enable signal. Updates are also applied only to the content of the first register 120, the type of update preferably being dependent on content of the control register for the particular address that is in the first register 120."

A6

Please replace the paragraph beginning on page 12, lines 1-12 with the following rewritten paragraph:

"A data processing device has load and store instructions which address memory with the content of a data pointer register. In a normal mode, the same data pointer register is used for all load and store instructions. In this mode the processor is compatible with a older processor design. In a special mode, at least two different registers are used alternately to address memory when memory access instructions are executed. A control register controls whether or not the different registers are updated as part of the memory access instructions. Preferably, the control register provides for more than one different kind of update of the different registers, such as post addressing increment, post addressing decrement etc."

A7